REMARKS

Claims 1-41 are pending in this application. Claims 11-18 and 30-39 have been finally withdrawn from consideration by the restriction requirement.

The Pending Objection and Rejection

The Office has objected to the drawings for the reasons set forth on pages 2-3 of the Office Action of May 1, 2003. The Office has also rejected claims 1-10, 19-29, and 40-41 under 35 U.S.C. § 112, ¶ 1 as containing non-enabled subject matter for the reasons listed on pages 2-3 of the same Office Action. Applicant respectfully traverses both this objection to the drawings and this enablement rejection.

The objection to the drawings and the rejection of the pending claims appear to be the proverbial "two sides of the same coin." On page 3 of the Office Action, the Office takes the position that the drawings do not show—and the specification does not enable—a field transistor that does not contain a gate insulating layer. Viewing Figure 2, the Office argues that layer 170 is an insulating layer and, as known in the art, since it is located above a channel, between a source and drain, and is directly below a gate, layer 170 must therefore be a gate insulating layer.

The Office's argument, however, fails to consider an important principle of how terms in a claim are to be analyzed. In analyzing the claims, the terms must be read in light of what the specification would have conveyed to one with ordinary skill in the art. In the specification of the present application, there is a clear indication of what the skilled artisan would have understood these claim terms to mean.

When discussing the prior art device depicted in Figure 1, the present specification refers to a field oxide layer 17 and a gate insulating layer 19. *See Specification, ¶ 05-06, 08.* Based on his knowledge and this description, the skilled artisan would have understood that the "thick" field oxide layer 17 (highlighted in pink in Exhibit A) could be a conventional isolation layer, i.e., a LOCOS (LOCal Oxidation of Silicon) layer. As well, when looking at the prior art device indicated in Figure 1, the skilled artisan would have understood the "thin" layer 19 between the gate conductor layer 18 and the source region 14 (as well as between the gate conductor layer 18 and the drain region 15) to be a gate insulating layer (highlighted in yellow in Exhibit A).

Figure 2 depicts a device in one aspect of the present invention. When discussing Figure 2, the specification refers to layer 170 as a field oxide layer (highlighted in pink in Exhibit B). *See also Specification, ¶ 30-31.* A side-by-side comparison of Figure 1 and 2 illustrates to the skilled artisan the differences (and similarities) between the devices of the prior art (Figure 1) and the device of the invention illustrated in Figure 2. One of such similarities is the existence of a field oxide layer (17 in Figure 1; 170 in Figure 2). One of such differences is the presence of a gate insulating layer 19 in Figure 1 and the absence of a corresponding gate insulating layer in Figure 2. Thus, in light of the specification and Figures 1 and 2, the skilled artisan would have been lead to one inescapable conclusion: the field transistors of the invention (unlike the prior art) while containing a thick field oxide layer, do not contain a gate insulating layer.

Such a conclusion is explicitly confirmed near the end of paragraph 11 and the first sentence of paragraph 33 of the present specification. In these two paragraphs, the specification refers to a "thin" gate insulating layer for comparison purposes against the "thick" field oxide layer. *See Specification, ¶ 08.*

Following the Office's arguments detailed in the Office Action of May 1, 2003 to their logical conclusion would lead the skilled artisan to conclude that the layer 170 in Figure 2 is a gate insulating layer. Yet the present specification explicitly and repeatedly refers to layer 170 as a field oxide layer. Thus, the Office's position would have the skilled artisan completely ignore the specification of the present application.

Despite the above arguments, Applicant has opted to amend the claims as indicated above solely in an effort to expedite prosecution. It appears from paragraph 2 of the Office Action of May 1, 2003 that the Office believes that a thick gate insulator is shown in Figure 2 and, therefore, that Figure 2 does depict a field transistor not having a thin gate insulating layer. To that end, Applicant has amended the claims as indicated above.

Accordingly, Applicant respectfully requests withdrawal of this objection to the drawings and rejection of the claims.

CONCLUSION

For the above reasons, as well as those of record, Applicant respectfully requests the Office to withdraw the pending grounds of rejection and allow the pending claims.

If there is any fee due in connection with the filing of this Amendment, including a fee for any extension of time not accounted for above, please charge the fee to our Deposit Account No. 50-0843.

CUSTOMER NUMBER

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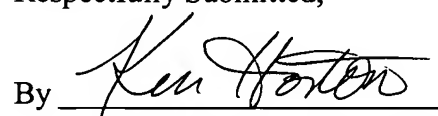
Respectfully Submitted,

By 

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